REMARKS

Claims 1-4 are all the claims pending in the application.

The Examiner rejects claims 1-4 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 5,602,509 to Kimura. Applicant respectfully traverses this rejection. Kimura does not disclose or suggest all of the features of Applicant's invention as claimed in independent claims 1 and 3.

For example, one of the features of Applicant's invention as claimed in claims 1 and 3 is "drain electrodes of said first and second MOS transistors forming output terminals for outputting a signal to be subtracted, and source electrodes of said first and second MOS transistors being commonly coupled to form an output terminal outputting a voltage to be added". The Examiner alleges that transistors M56 and M57 of Fig. 1 of Kimura correspond to the first and second transistors of Applicant's claimed invention. Applicant respectfully disagrees.

First, the circuit in Fig. 1 of Kimura cannot function as an adder/subtractor circuit because it outputs a current, not a voltage, as the claim requires. The Examiner alleges that it would have been obvious to use a resistor to convert this current into a voltage. Applicant disagrees. It would not be obvious that a resistor would be sufficient to convert the output current into a voltage equal to the difference in voltage of the input signals. According to Ohm's law, the resulting voltage would be different depending on the size of the resistor, and therefore would not represent the difference between the input voltages. It is likely that a much more

elaborate voltage converter circuit would be needed, but the details of such a circuit are not obvious and are not disclosed by Kimura. At least for this reason, Kimura does not disclose or suggest a "source electrodes of said first and second MOS transistors being commonly coupled to form an output terminal outputting a voltage" as required by Applicant's claimed invention.

Second, Kimura does not disclose that the source electrodes of its transistors M56 and M57 are commonly coupled to form an "output terminal of a voltage to be added" as required by claims 1 and 3. Kimura describes only that the source of M56 and M57 are connected. The Examiner assumes that because Kimura discloses that transistors M56 and M57 compose a differential pair, these transistors form a subtractor circuit. Even if, assuming *arguendo*, transistors M56 and M57 form a subtractor circuit, Kimura does not disclose or suggest that these transistors have commonly connected drains that form a voltage adder circuit with an addition output terminal as the claim requires.

Furthermore, the Examiner has misinterpreted the function of the circuit of Kimura. When the circuit of Kimura becomes as an OTA operating linearly (i.e. when n=2.157) (Kimura, column 3, lines 53-60) the voltage at node B becomes (V1+V2)/2-V0. But because V0 is a constant voltage, the voltage of node B becomes a level shifted version proportional to the addition voltage. Furthermore, through a current level shifter M55, a current flows that is equal to a constant current aI from which a current proportional to the square of an input voltage, i.e., (V1-V2)2, is subtracted. Therefore, the voltage at node A becomes a voltage which is an addition of a level shifted voltage of the node B voltage and a voltage proportional to the absolute value of an input voltage (V1-V2), i.e., [V1-V2]. That is, the voltage at node A does not become an

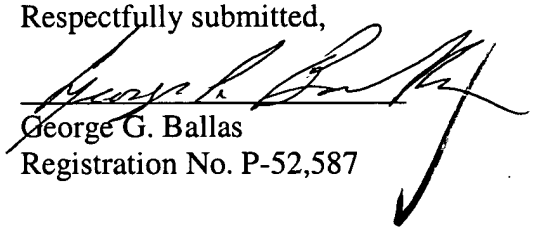
addition of input voltages, but becomes a level shifted voltage of a voltage proportional to the absolute value of a difference between applied voltages. Thus, the circuit shown in Fig. 1 of Kimura can not accomplish the function of Applicant's invention as claimed in claim 1.

Because Kimura does not disclose or suggest at least the above-noted features of Applicant's invention as claimed in claims 1 and 3, claims 1 and 3 are not anticipated by (i.e., do not read on) Kimura. Claims 2 and 4 are allowable at least by virtue of their dependence on claims 1 and 3, respectively.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned attorney at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



George G. Ballas
Registration No. P-52,587

SUGHRUE MION, PLLC
Telephone: (202) 293-7060
Facsimile: (202) 293-7860

WASHINGTON OFFICE

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